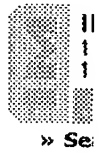




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1 Technology mapping for simultaneous gate and interconnect optimisation

Lü, A.; Stenz, G.; Eisenmann, H.; Johannes, F.M.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 146 , Issue: 1 , Jan. 1999

Pages:21 - 31

[\[Abstract\]](#) [\[PDF Full-Text \(1124 KB\)\]](#) **IEEE JNL**

2 A technology mapper for Xilinx FPGAs

Chikodikar, M.Y.; Laddha, S.; Sirasao, A.;

VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan 1997

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3 A comparing study of technology mapping for FPGA

Martin, H.-G.; Rosenstiel, W.;

Design, Automation and Test in Europe, 1998., Proceedings , 23-26 Feb. 1998
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[Abstract] [PDF Full-Text (16 KB)] IEEE CNF

4 Non-disjoint decomposition of Boolean functions and its application FPGA-oriented technology mapping

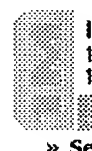
Rawski, M.; Jozwiak, L.; Nowicka, M.; Luba, T.;

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